HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Docket No.: 10971353-3
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
David P. Hannum et al.

Application No.: 10/687,907 Confirmation No.: 1941

Filed: October 17, 2003 Art Unit: 2185

For: SYSTEM AND METHOD FOR RESETTING AND INITIALIZING AN ALAT TO A KNOWN STATE AT POWER ON OR THROUGH A MACHINE SPECIFIC STATE

Examiner: D. Tran

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.41(a)(1), this Reply Brief is filed within two months of the Examiner's Answer dated April 20, 2006, and is in furtherance of said the Appeal Brief filed on November 10, 2005.

No fee is required for this REPLY BRIEF.

This brief contains items under the following headings pursuant to M.P.E.P. § 1208:

I. Status of Claims
II Grounds of Rejection to be Reviewed on Appeal
III. Argument
IV. Conclusion

I. STATUS OF CLAIMS

Claims 1-3, 6-13, and 16-19 are pending in the current application and are now on appeal.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2, 7, 8, 10-12, and 17-19 are rejected under 35 U.S.C. § 102(b) as being anticipated by Miller et al. (U.S. Patent No. 5,509,528, hereinafter *Miller*).

Claims 6, 9, and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Miller* in view of Geva (U.S. Patent No. 6,539,541, hereinafter *Geva*).

Claims 3 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Miller* in view of Hale et al. (U.S. Patent No. 6,564,317, hereinafter *Hale*).

III. ARGUMENT

This Reply Brief addresses the arguments raised by the Examiner in the Examiner's Answer, mailed April 20, 2006. *See* Examiner's Answer at pages 11-18. Appellant's Appeal Brief filed on November 10, 2005 is hereby incorporated by reference. For the convenience of the Board, Appellant has followed the same paragraph numbering used by the Examiner in the Response to Argument section of the Examiner's Answer.

1. In response to the Examiner's obviousness-type double patenting rejection, Appellant reasserts that it will file a Terminal Disclaimer that will be in compliance with 37 C.F.R. § 1.321(b), if this rejection still properly stands, upon an indication of allowability on all other matters.

2. Contrary to the Examiner's arguments, *Miller*'s invalid state is not the same limitation as the claimed illegal values. As noted in the Appeal Brief, *Miller* explicitly defines an invalid value as a non-current, old or stale value. *Miller* at col. 15, lns. 19-23. Thus, by definition, *Miller*'s invalid state is acquired during the normal course of program execution. Meanwhile, the claimed illegal value is defined as "a value . . . not acquire[d] in a

normal course of program execution." Present Specification at page 8, lns. 21-22. Therefore, *Miller*'s invalid state is not the same limitation as the claimed illegal values, at least, because *Miller*'s invalid state is acquired during normal program execution, whereas the claimed illegal value is not.

In response to the above remarks, the Examiner argues that *Miller*'s "initialization" is not part of the normal course of program execution. Examiner's answer at page 12. In other words, the Examiner contends that *Miller*'s values are not acquired during the normal course of program execution because they are acquired during initialization. *Id.* However, even assuming, *arguendo*, that initialization is not part of the normal course of program execution, the mere fact that a value is acquired during initialization does not mean that the same value is not also acquired during the normal course of program execution. In fact, as noted above, *Miller* teaches that the invalid values acquired during initialization indeed are also acquired during the normal course of program execution, for example, when values become old, non-current, or stale. *Miller* at col. 15, lns. 19-23. Therefore, *Miller*'s invalid state is not the same limitation as the claimed illegal values.

3. The Examiner contends that "'non-current,' 'stale,' and 'old' data is not a normal situation in a computer system . . . ," thus *Miller*'s invalid state is not acquired during the normal course of program execution. Examiner's Answer at page 14. Appellant respectfully disagrees. While *Miller* may describe "non-current," "stale," and "old" data as undesirable (*Miller* at col. 3, lines 29-41), it recognizes that this is indeed a "normal situation." For example, at the very passage cited by the Examiner, *Miller* teaches that

> [c]ache memory information becomes invalid, stale or old when it has been modified in some areas of memory and not in others. For example, in a multi-processor system, information originally stored in main memory may be modified by another processor and, in that case, the information stored in a another cache memory would no longer be current. Because it is no longer current, the data is referred to as old, stale or invalid.

Miller at col. 3, lines 17-22. Therefore, the process by which data becomes "non-current," "stale," and "old" occurs during normal operation of program execution, for example, in a multi-processor system. Again, *Miller*'s invalid state is not the same limitation as the

claimed illegal values, at least, because an invalid state is acquired during normal program execution, whereas an illegal value is not.

4. Contrary to the Examiner's arguments, *Miller* does not teach or suggest the claimed force update command. At the first passage cited by the Examiner, *Miller* simply teaches a system initialization procedure. *Miller* at col. 15, lns. 35-50. *Miller*'s initialization procedure does not include a force update command for causing a plurality of entry locations to acquire predetermined illegal bit values, at least, because *Miller* does not teach or even suggest illegal bit values. At the second passage cited by Examiner, *Miller* teaches a snoop operation for identifying an invalid entry (*i.e.*, an entry containing a non-current, stale or old value) and for setting a flag to indicate that the entry is invalid. *Miller* at col. 3, lns. 21-24; col. 16, lns. 11-15. However, an operation that merely identifies an invalid entry is not a force update command. And, again, *Miller*'s invalid entry is not the same as an illegal entry. Therefore, neither of *Miller*'s system initialization procedure nor *Miller*'s operation for identifying an invalid table entry and setting an invalid entry flag are a force update command for causing entry locations to acquire predetermined illegal bit values.

5 and 6. There is no suggestion or motivation to combine the teachings of *Miller* and *Geva*. The Examiner contends that:

> [i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Geva into the system of Miller because it would allow handling advanced loads in a cache system; thereby increasing the performance and speed processing of the system.

Examiner's Answer at page 16. Appellants point out that *Miller* discloses a method of handling invalid data in a cache memory system, whereas *Geva* teaches a method for compiling loop instructions. *See Miller* at col. 1, lns. 8-12; *Geva* at col. 4, lns. 25-38. There is simply no suggestion either in the references themselves or in the knowledge generally available to one of ordinary skill in the art that *Miller*'s method for handling invalid data in a memory is combinable with, or would benefit from, *Geva*'s method of compiling a loop instruction, and the Examiner has not show otherwise.

Moreover, a prima facie case of obviousness has been established because the Examiner has not provided an objective reason to combine the teachings of the references. Particularly, the motivation put forth by the Examiner—*i.e.*, for "increasing the performance and speed processing of the system," is a general incentive, and not an objective reason to combine the references. Appellant points out that "[a] general incentive does not make obvious a particular result, nor does the existence of techniques by which those efforts can be carried out." *In re Deuel*, 51 F.3d 1552, 1559 (Fed. Cir. 1995). Therefore, the motivation for the combination of *Miller* and *Geva* is improper.

7 and 8. There is no suggestion or motivation to combine the teachings of *Miller* and *Hale*. The Examiner contends that:

> [i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hale into the system of Miller because it would allow a secure boot process when performing initialization of a computer system upon power up or system reset. Final Office Action, page 6.

Examiner's Answer at page 18. Appellants point out that *Miller* discloses a method of handling invalid data in a cache memory system, whereas *Hale* teaches a method for securing computer firmware during initialization. *See Miller* at col. 1, lns. 8-12; *Hale* at Abstract. There is simply no suggestion either in the references themselves or in the knowledge generally available to one of ordinary skill in the art that *Miller*'s method for handling invalid data in a memory is combinable with, or would benefit from, *Hale*'s method for securing computer firmware during initialization, and the Examiner has not shown otherwise.

Moreover, a prima facie case of obviousness has been established because the Examiner has not provided an objective reason to combine the teachings of the references. Particularly, the motivation put forth by the Examiner—*i.e.*, for "increasing the performance and speed processing of the system," is a general incentive, and not an objective reason to combine the references. Appellant points out that "[a] general incentive does not make obvious a particular result, nor does the existence of techniques by which those efforts can be carried out." *In re Deuel*, 51 F.3d 1552, 1559 (Fed. Cir. 1995). Therefore, the motivation for the combination of *Miller* and *Geva* is improper.

IV. CONCLUSION

Appellant respectfully requests that the Board reverse the outstanding rejections of pending claims 1-3, 6-13, and 16-19 for the above reasons.

Dated: June 19, 2006

Respectfully submitted,

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Dated: June 19, 2006

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06-20-06

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PATENT APPLICATION

ATTORNEY DOCKET NO. 10971353-3

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TRANSMITTAL OF REPLY BRIEF

Transmitted herewith is the Reply Brief with respect to the Examiner's Answer mailed on April 20, 2006.

This Reply Brief is being filed pursuant to 37 CFR 1.193(b) within two months of the date of the Examiner's Answer.

(Note: Extensions of time are not allowed under 37 CFR 1.136(a))

(Note: Failure to file a Reply Brief will result in dismissal of the Appeal as to the claims made subject to an expressly stated new ground rejection.)

No fee is required for filing of this Reply Brief.

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Respectfully submitted,
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Application No.: 10/687,907 Attorney Docket No.: 10971353-3

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